## Remarks

This Amendment is responsive to the Office Action of November 3, 2005. Reexamination and reconsideration of claims 1-44 is respectfully requested.

## Summary of The Office Action

Claims 1, 3, 6-16, 29-30 and 32-34 were rejected under 35 U.S.C. §102(b) as being anticipated by Jeddeloh (U.S. Pat. No. 6,363,502).

Claim 2 was rejected under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh and Frisch (U.S. Pat. No. 5,721,828).

Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh and Vivio et al. (U.S. Pat. No. 5,867,642).

Claims 17-19, 21-28, 35-38, and 40-44 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh and Vivio and further in view of Nguyen et al. (U.S. PGPub No. 20040143719).

Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh and Chauvel et al. (U.S. PGPub No. 20040024970).

Claims 20 and 39 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh and Vivio and Nguyen and further in view of Chauvel.

Claim 31 was rejected under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh and Mellor et al. (U.S. PGPub No. 20040169885).

**The Claims Patentably Distinguish Over the References**

Claims 1, 3, 6-16, 29-30 and 32-34 were rejected under 35 U.S.C. §102(b) as being anticipated by Jeddeloh (U.S. Pat. No. 6,363,502).

**35 U.S.C. §102**

For a 35 U.S.C. §102 reference to anticipate a claim, the reference must teach every element of the claim. Section 2133 of the MPEP recites:

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Here, Jeddeloh does not teach every element of the claim.

Jeddeloh discloses a system in which sub-standard memory can be used. An error handler will be selected on a per i/o (e.g., read, write) basis. Since sub-standard memory can be used, multiple error handlers are available. Error handler selection will involve the processor in the system. The selection will involve a remapping table. However, simply having a remapping table does not anticipate the claims.

The application and claims describe logically replacing a first memory location with a second memory location and then testing the first memory location for memory errors. The testing occurs independent of the central processor in a system in which the memory resides. The testing also occurs independent of any operating system running on the system in which the memory resides. The testing also occurs independent of the second location being used.

While Jeddeloh may describe mirrored memory locations, no testing of the logically replaced location occurs. For this reason Jeddeloh does not anticipate any of the claims.

Independent Claim 1

As noted above, Jeddeloh does not teach "memory testing of the first memory location." Since Jeddeloh does not teach the testing, Jeddeloh also does not teach initiating the memory testing. Additionally, Jeddeloh does not teach controlling "copying contents between a first memory location and a second memory location". While memory reads and writes may occur,

there is no copying from a first memory location to a second memory location so that the first location can be tested without interfering with either the processor or the operating system.

Additionally, the Office Action asserts that the reference teaches the memory quality assurance logic being configured to control copying contents. The Office Action supports this assertion by reciting that "the processor access a remapping table". If the processor is taking the action, then the memory quality assurance logic is not taking the action.

Additionally, the Office Action asserts that the reference teaches the memory quality assurance logic being configured to initiate memory testing. The Office Action supports this assertion by reciting that "the processor then accesses the remapped memory portion and performs the requested operation." However, the requested operation is not memory testing. The requested operation is a read or write.

Since claim 1 recites features not taught or suggested by the reference, claim 1 patentably distinguishes over the reference. Accordingly, dependent claims 2-16 also patentably distinguish over the reference and are allowable.

Dependent Claim 3

Claim 3 recites the additional element of the memory mapping logic including an address translation table(s). Jeddeloh describes a remapping table. The remapping table is not the same as an address translation table that performs physical to logical address translation like that claimed and described. The remapping table simply diverts one physical address to a different physical address. There is no physical/virtual translation. For this additional reason this claim is allowable.

Dependent Claim 6

Claim 6 recites the additional element of the memory quality assurance logic being configured to selectively logically replace the first memory location with the second memory location ... based, at least in part, on a result from the memory testing of the first memory location. Since the first memory location is never tested, no selective replacement can occur based on testing that does not occur. For this additional reason this claim is allowable.

Dependent Claim 7

Claim 7 recites the additional element of the memory quality assurance logic being configured to selectively logically replace the first memory location with another memory location ... based, at least in part, on a result from the memory testing of the first memory location. Since the first memory location is never tested, no selective replacement can occur based on testing that does not occur. For this additional reason this claim is allowable.

Dependent Claim 8

Claim 8 recites the additional element of the memory quality assurance logic being configured to initiate memory testing ... by sending ... signals to a memory testing logic. Once again the reference does not describe testing the first memory location. Thus, no signals to start this testing that does not occur are ever sent. The Office Action asserts that the claimed element is described and supports the assertion by reciting "the memory controller processor employs the controls lines to inform a selected ... error detection ... module whether the memory access includes a read or write." Simply telling an error detection module whether an i/o is a read or write is not the same as initiating testing. Informing and controlling are different things. A process can inform an error handler whether an i/o is a read or write without causing any testing to be initiated. For this additional reason this claim is allowable.

Dependent Claim 9

Claim 9 recites the additional element of the memory quality assurance logic being configured to initiate memory testing ... by sending ... signals to a memory testing logic. Once again the first memory location is never tested by the systems and methods described in the reference. Thus, no signals to start this testing that does not occur are ever sent. For this additional reason this claim is allowable.

Dependent Claim 10

Claim 10 recites the additional element of the quality assurance logic selecting the second memory location. In the reference no copying occurs. Thus no second location is selected. For this additional reason this claim is allowable.

Dependent Claim 11

Claim 11 recites the additional element of the quality assurance logic including data stores that store data like memory freshness, memory quality, and so on. The reference describes configuration registers that store data concerning which error handling module to employ to support a read or write. A program entry point stored in a configuration register is not the same as any of the listed data types in claim 11. For this additional reason this claim is allowable.

Dependent Claim 12

Claim 12 recites the additional element of the quality assurance logic being connected to data stores that store data like memory freshness, memory quality, and so on. The reference describes configuration registers that store data concerning which error handling module to employ to support a read or write. A program entry point stored in a configuration register is not the same as any of the listed data types in claim 12. For this additional reason this claim is allowable.

Dependent Claim 13

Claim 13 recites the additional element of the second memory location being internal to the memory mapping logic. The Office Action previously identified the processor as being the memory mapping logic. The Office Action then asserts that items 12A and 13A-20A teach the second memory location being internal to the memory mapping logic. Items 12A and 13A-20A are clearly not internal to the processor. Indeed, they are not internal to any element except the memory module. For this additional reason this claim is allowable.

Dependent Claim 14

Claim 14 recites the additional element of the second memory location being internal to the memory quality assurance logic. The Office Action previously identified the processor as being the memory quality assurance logic. The Office Action then asserts that items 12A and 13A-20A teach the second memory location being internal to the memory quality assurance logic. Items 12A and 13A-20A are clearly not internal to the processor. Indeed, they are not internal to any element except the memory module. For this additional reason this claim is allowable.

Dependent Claim 16

Claim 16 recites the additional element of the memory quality assurance logic being configured to select the second memory location. Once again, no contents are copied in the reference and thus no second location is selected. For this additional reason this claim is allowable.

Independent Claim 29

Claim 29 is rejected using the same rationale as for claim 1. However, as described above, Jeddeloh does not teach remapping a location so that the remapped location can be tested. Jeddeloh discloses a remapping table, but the remapping table is not employed to free up a location for independent, parallel testing. To the extent that any testing is described in Jeddeloh, it is performed on a per read/write basis on the new location, not on the remapped location. For at least this reason and for the reasons explained in connection with claim1, claim 29 is allowable. Accordingly, dependent claims 30-34 are also allowable.

Dependent Claim 32

Claim 32 recites the additional element of the memory quality assurance logic including data stores that store data like memory freshness, memory quality, and so on. The reference describes configuration registers that store data concerning which error handling module to employ to support a read or write. A program entry point stored in a configuration register is not the same as any of the listed data types in claim 32. For this additional reason this claim is allowable.

Dependent Claim 33

Claim 33 recites the additional element of the quality assurance logic being connected to data stores that store data like memory freshness, memory quality, and so on. The reference describes configuration registers that store data concerning which error handling module to employ to support a read or write. A program entry point stored in a configuration register is not the same as any of the listed data types in claim 33. For this additional reason this claim is allowable.

**35 U.S.C. §103**

To establish a prima facie case of 35 U.S.C. §103 obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. MPEP 2143.01 Second, there must be a reasonable expectation of success. MPEP 2143.02 Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143.03 Additionally, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). This requirement is intended to prevent unacceptable "hindsight reconstruction" where Applicant's invention is recreated from references using the Application as a blueprint.

Here, the third criteria described in MPEP 2143.03 is not satisfied since the reference (and/or combination of references) does not teach or suggest all the claim limitations. None of the references, alone and/or in combination, teach copying the contents of a first memory location to a second memory location and then testing the first memory location without disturbing an operating system or consuming processor cycles allocated to regular processing. Thus, none of the claims are obvious for at least this reason.

Dependent Claim 2

Claim 2 was rejected under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh and Frisch. As described above, Jeddeloh does not describe every element of claim 1, from which claim 2 depends. Frisch does not remedy the defects of Jedelloh.

Claim 2 recites the additional element of the system including a crossbar. While Frisch describes a crossbar, it is not the type of crossbar claimed. Frisch describes a crossbar that connects nodes in a multiprocessing system. This is not the type of crossbar claimed. For this additional reason this claim is allowable.

Dependent Claim 5

Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh and Vivio. As described above, Jeddeloh does not describe every element of claim 1, from which claim 5 depends. Vivio does not remedy the defects of Jedelloh.

Claim 5 recites the additional element of the system being "configured to selectively logically remove the first memory location ... based ... on a result from the memory testing of the first memory location." Neither Jeddeloh nor Vivio describe testing a first memory location that has been mirrored in a second location and then logically removed from the available memory pool. Thus, neither Jeddeloh nor Vivo describe taking an action based on the result of the testing that never occurred. For this additional reason this claim is allowable.

Claims 17-19, 21-28, 35-38, and 40-44 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh and Vivio and further in view of Nguyen.

Independent Claim 17

Claim 17 recites "initiating memory testing of the first memory location without an operating system interaction." There are two elements in this claim that are not found in any of the references. None of the references, alone or in combination teach memory testing the first memory location. Additionally, to the extent that any testing is performed by any of the references, it clearly involves an operating system interaction.

The Office Action asserts that Nguyen teaches memory testing without an operating system interaction. The Office Action references [0024], which reads, "memory testing may be performed ... in a system management mode ... as may be triggered by ASM 36 ... and thus the testing may be transparent to the operating system." However, this statement is internally inconsistent with the rest of the application. In fact, the rest of the application makes it abundantly clear that not only does the testing include an operating system interaction, but that the interaction is to **completely halt the operating system**. It is hard to imagine what could be a bigger operating system interaction.

Consider paragraph [0020], which reads, "The computer system 100 may also comprise an advanced server management (ASM) device 36 ... the ASM 36 may be responsible for

issuing system management interrupts to the processors 2 ... Upon receiving an SMI, the processors 2 may **suspend execution of the operating system.**" (emphasis added).

Consider also paragraph [0028], which reads, "upon receiving the system management interrupt, the processors 2 may **suspend execution of the operating system.**" (emphasis added). Thus, although the reference in paragraph [0024] asserts that its testing is transparent to the operating system, this assertion is sandwiched by directly contradictory statements. Therefore the reference does not support the Office Action assertion, and this claim is allowable.

Accordingly, dependent claims 18-28 are also allowable.

Dependent Claim 18

Claim 18 recites the additional element of being able to access the contents copied from the first location to the second location while the first location is being memory tested. None of the references describe testing the first location and thus none of them describe this parallel aspect. For this additional reason this claim is allowable.

Dependent Claim 19

Claim 19 recites the additional element of being able to test the first memory location without consuming a non-memory operating system resource. The Office Action asserts that Vivio discloses this element. The Office Action refers to a portion of Vivio that recites that the testing will occur "without affecting system operation or denying other applications or devices from accessing memory **for an extended period of time.**" (emphasis added). Thus, rather than supporting the assertion, this passage actually indicates that system operation will be halted for at least a short period of time. For this additional reason this claim is allowable.

Dependent Claim 24

Claim 24 recites the additional element of providing a report concerning a quality of the first memory location. The Office Action asserts that Jeddeloh discloses providing this report by disclosing that "a processor ... determines whether an error correction code, known as the syndrome, indicates that there is an error in the memory portion that was read." However, the "memory portion that was read" is not the first memory location. In Jedelloh, the read/write operations are performed on the second memory location while the first memory location is left

alone. Thus, to the extent than Jeddeloh provides any report, it provides it concerning the second memory location, not the first memory location. For this additional reason this claim is allowable.

Dependent Claim 25

Claim 25 recites the additional element of storing quality data concerning the first memory location, where the quality data is based on testing the first location. None of the references, alone or in combination, disclose testing the first location. To the extent that any testing is done, it is done on the second location during read/write operations. For this additional reason this claim is allowable.

Dependent Claim 27

Claim 27 recites the additional element of the first memory location being tested by a variety of testing methods. The Office Action relies on paragraph [0025] of Nguyen to support the rejection. However, this paragraph describes how the testing directly impacts the system because the processor is involved in the testing. If the disclosed method is consuming processor cycles then it is most certainly not transparent and it is most certainly interacting with the operating system by, for example, slowing it down because it can't execute when the testing occurs. For this additional reason this claim is allowable.

Independent Claim 35

Claim 35 recites a computer readable medium that stores processor executable instructions operable to perform a method like that claimed in claim 17. The Office Action tersely recites that "Claim 35 is rejected using the same rationale as for the rejection of claim 17 above." However, claim 17 is not a computer readable medium claim.

The Office Action does not assert that any of the references disclose the method claimed in claim 35 as being stored on a computer readable medium. For this additional reason this claim is allowable.

Accordingly, dependent claim 36 is also allowable.

Independent Claim 37

Claim 37 is a means plus function claim that recites three separate times that actions are performed without interacting with an operating system. As illustrated above, all of the references interact with an operating system. In particular, Nguyen claims that it does not interact with an operating system then explains how it **halts** the operating system. For at least this reason claim 37 is allowable.

Independent Claim 38

Claim 38 describes an "operating system transparent system for on-the-fly memory testing". As illustrated above, all of the references interact with an operating system. In particular, Nguyen claims that it does not interact with an operating system then explains how it actually **halts** the operating system. For at least this reason claim 38 is allowable.

Accordingly, dependent claims 39-43 are also allowable.

Dependent Claim 40

Claim 40 recites the additional element of the programmable memory address resolving logic including a crossbar and/or an address translation table. No crossbar appears in any of Jedelloh, Vivio, and Nguyen. While an irrelevant crossbar appears in Frisch, claim 40 is not rejected in light of Frisch, and thus this rejection should be removed.

Dependent Claim 42

Claim 42 specifically recites that the memory location can be logically removed without requiring an operating system to halt execution. However, both paragraphs [0020] and [0028] in Nguyen specifically point out that the testing will "**suspend execution of the operating system.**" (emphasis added). The Examiner is invited to explain how a system that will suspend execution of the operating system makes obvious a claim that recites not suspending execution of an operating system.

Independent Claim 44

Claim 44 specifically recites that the memory location can be tested "without disrupting an operating system instance". However, both paragraphs [0020] and [0028] of Nguyen

specifically point out that the testing will "**suspend execution of the operating system.**" (emphasis added). The Examiner is invited to explain how a system that will suspend execution of the operating system makes obvious a claim that recites not disrupting an operating system.

Claim 4

Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh and Chauvel. As described above in connection with claim 1, from which claim 4 depends, Jeddeloh does not anticipate or make obvious claim 1. Chauvel does not remedy the defects of Jeddeloh. Thus claim 4 is similarly not anticipated and not made obvious. Additionally, claim 4 recites the memory quality assurance logic using various methods to select a memory location to test. While Chauvel describes using some of the claimed methods for memory management, neither Chauvel nor Jeddeloh describe using these methods to select a location to test. For this additional reason this claim is allowable.

Claims 20 and 39

Claims 20 and 39 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh and Vivio and Nguyen and further in view of Chauvel. The Office Action employs four references to make this "stretch rejection". In addition to be a stretch, this rejection is an impermissible application of hindsight reconstruction.

Concerning hindsight reconstruction, MPEP §2143 reads: the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicant will now comment on the propriety of combining four references in the manner performed in the Office Action. This appears to be hindsight reconstruction where the Office Action is using the Application as a blueprint to find parts of the claimed invention in unrelated references. Hindsight reconstruction has long been frowned upon:

> A rejection based on section 103 clearly must rest on a factual basis, and these facts must be interpreted without **hindsight reconstruction** of the invention from the prior art. In making this evaluation, all facts must be considered. The Patent Office has the initial duty of supplying the factual basis for its rejection. It may not, because it may doubt that the invention is patentable, resort to speculation, unfounded assumptions or **hindsight**

> **reconstruction** to supply deficiencies in its factual basis. In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968) (emphases in original).
>
> The mere fact that references <u>can</u> be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). MPEP 2143.01

The hindsight reconstruction engaged in by the Office Action is impermissible since nothing in the prior art or the references suggests the desirability of combining the four references. Above and beyond being impermissible hindsight reconstruction, these references are fundamentally flawed in that the combination of references still does not teach every element of the claims.

Specifically, the combination of references does not teach identifying a memory location to test using the described methods, testing the location, and doing all of this without an operating system interaction or without consuming operating system resources.

Claim 31

Claim 31 was rejected under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh and Mellor. The Office Action asserts that the abstract in Mellor describes storing print job data in the memory of an image forming device. Applicant has read and re-read the abstract and finds no mention of print job data or of an image forming device. The Abstract reads:

> Memory management. A method embodiment includes receiving data separable into segments. For each segment, it is determined whether to save that segment to a first memory such as RAM or to a second memory such as a hard disk. Each segment is saved to a determined location. While saving each segment determined to be saved to the first memory, it is determined whether the first memory is depleted. When the first memory is determined to be depleted, a segment being saved to the first memory is instead saved to the second memory.

The Examiner is invited to point out the section of this Abstract that describes storing print job data. Regardless of this error in the Office Action, even if the Mellor abstract did describe storing print job data, this does not remedy the problems with Jedelloh nor does it teach doing the claimed memory testing in an image forming device. Simply storing print job data in

an image forming device is not equivalent to doing the type of memory testing claimed. For this additional reason this claim is allowable.

**Ascertaining Skill Level of One Skilled In The Art**

The MPEP requires that the Office Action ascertain and describe the level of ordinary skill so that objectivity can be maintained. MPEP §2141.03 reads:

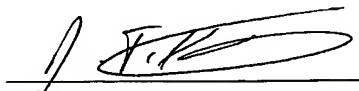
> The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry. *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718, 21 USPQ2d 1053, 1057 (Fed. Cir. 1991). The examiner must ascertain what would have been obvious to one of ordinary skill in the art at the time the invention was made, and not to the inventor, a judge, a layman, those skilled in remote arts, or to geniuses in the art at hand. *Environmental Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 218 USPQ 865 (Fed. Cir. 1983), *cert. denied*, 464 U.S. 1043 (1984).

Here the Office Action neither ascertains nor reports on the level of ordinary skill in the art. For this additional reason all the obviousness rejections are improper.

**Conclusion**

For the reasons set forth above, claims 1-44 patentably and unobviously distinguish over the references and are in condition for allowance. An early allowance of all claims is earnestly solicited.

Respectfully submitted,



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